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Verilog-A implementation of a double-gate junctionless compact model for DC circuit simulations

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Received 5 March 2016
Accepted for publication 20 April 2016
Published 31 May 2016

Abstract
A physically based model of the double-gate junctionless transistor which is capable of describing accumulation and depletion regions is implemented in Verilog-A in order to perform DC circuit simulations. Analytical description of the difference of potentials between the center and the surface of the silicon layer allows the determination of the mobile charges. Furthermore, mobility degradation, series resistance, as well as threshold voltage roll-off, drain saturation voltage, channel shortening and velocity saturation are also considered. In order to provide this model to all of the community, the implementation of this model is performed in Ngspice, which is a free circuit simulation with an ADMS interface to integrate Verilog-A models. Validation of the model implementation is done through 2D numerical simulations of transistors with m₁m₄ and 40 nm silicon channel length and 1 × 10¹⁹ or 5 × 10¹⁸ cm⁻³ doping concentration of the silicon layer with 10 and 15 nm silicon thickness. Good agreement between the numerical simulated behavior and model implementation is obtained, where only eight model parameters are used.

Keywords: junctionless transistors, compact modeling, Verilog-A, circuit simulation

(Some figures may appear in colour only in the online journal)

1. Introduction
Due to the uniformly doped nanowire without junctions, as well as a wrap-around gate, junctionless transistors (JLT) are one of the most promising candidates to cover the ITRS projections for 20 nm downscaling [1]. JLT transistors can be fabricated in a similar way to FinFETs transistors [1]. However, their behaviour can be basically related to a resistor in which the mobile carrier density can be modulated by the gate. As a result, a trade-off between a heavily doped and a thin silicon layer has to be made in order to increase the device conductivity, as well as to ensure a full depletion and current cut-off. Furthermore, similar to FinFETs, JLTs can work as Double Gate o Tri-Gate MOSFETs [2–6].

In order to simplify the analysis of its current-voltage behavior, a double-gate JLT (DJLT) has to be considered such as in [7–10], where numerical-analytical or complete analytical models are presented. Most models have been developed at different regions of operation [11–13] and a few for all regions [14–17]. It is worth pointing out that one of the main problems in the modeling of the DJLT is the transition from the depletion mode to accumulation mode, because of its different physical behaviors. The JLT is fully depleted below threshold voltage and the device is turned-off, as the gate voltage is increased, the electron concentration also increases until it reaches the threshold. If the gate voltage is increased further, the entire
cross-section of the transistor channel becomes neutral. As a result, the device is no longer depleted and the flat-band voltage is reached. In fully depleted as well as at partially depleted conditions, the current is defined by the charge transport at or near the center of the silicon layer (body current) [18]. However, for gate voltages larger than the flat-band condition, the accumulation mode is reached and an additional current starts to flow underneath the insulator while the body current remains.

Recently we presented a drain current model for DJLT considering the total mobile charge in the channel from the center to the surface [19]. Afterwards, short-channel effects were included as the increase of the body potentials due to the drain bias, mobility degradation, carrier velocity saturations and series resistance. In this paper we present the implementation of this analytical DJLT model in Verilog-A, which allows its introduction in commercial circuit simulators for circuit design. The implementation in Verilog-A is also validated using simulations in ATLAS [20].

2. Model description

2.1. Potentials

The 2D structure of the DJLT under analysis is shown in figure 1, where \( L \) is the gate length, \( W \) is the gate width, \( L_{\text{ext}} \) is the equivalent oxide thickness (EOT), \( t_s \) is the silicon thickness of the transistor and \( L_{\text{ext},s} \) is the silicon extension at source and drain, which have a higher doping concentration \( N_{\text{ext},s} \).

According to this 2D structure, the difference of the potentials of the silicon layer between the surface, \( \psi_s \), and the center, \( \psi_t \), normalized with respect to the thermal voltage, \( \psi_t \), can be calculated as shown in (1) according to [21].

\[
\alpha = \alpha_{\text{br}} + LW \left[ -\alpha_{\text{br}} \cdot e^{-\alpha_{\text{br}} \cdot \frac{\psi_s-V}{\psi_t}} \right]
\]

(1)

where \( \alpha_{\text{br}} \) is the normalized difference of potentials in deep subthreshold, \( V \) is the channel voltage and \( LW \) is the Lambert function. Furthermore, when a gate voltage, \( V_G \), and drain voltage, \( V_D \), are applied, they will affect the surface potential as:

\[
V_G - V_{FB} = \psi_s + \text{sign}(\alpha) \cdot \psi_t \cdot \beta \cdot e^{\frac{\psi_t - \psi_s}{\gamma}} - \xi \cdot \alpha - 1
\]

(2)

where \( \beta = \frac{q_\text{N}_t}{\sqrt{2} \cdot E_\text{v}} \), \( \xi = \left( 1 - \frac{1}{\alpha_{\text{br}}} \right) \), \( q_\text{b} = \frac{q_\text{N}_t}{C_{\text{ox}}} \) is the normalized fixed charge in the silicon layer, \( C_{\text{ox}} \) is the gate capacitance per unit area, \( C_s \) is the silicon capacitance per unit area and \( \gamma = \frac{C_{\text{ox}}}{C_s} \).

Since it is not possible to get an analytic solution for the surface potential in (2), an iterative solution is showed in [18], where a precision better than 0.01% is obtained with a maximum of two iterations.

Moreover, the normalized difference of potentials at the threshold voltage is equal to:

\[
\alpha_T = \frac{\alpha_{\text{br}}}{1 - \alpha_{\text{br}}} \left[ 1 - \alpha_{\text{br}} \left( 1 - \frac{1}{2q_\text{b}} \right)^2 \right]
\]

(3)

2.2. Mobile charges

Considering just one half of the channel, an analytical expression of the mobile charge from the center to the surface of the silicon layer as a function of the potentials is found through solving Poisson’s equation:

\[
q_t = -\text{sign}(\alpha) \cdot \beta \cdot \sqrt{e^\xi \alpha - \xi \cdot \alpha - 1} - \frac{q_\text{b}}{2}
\]

(4)

Since DJLT presents two regimes of operation: depletion and accumulation, the drain current, \( I_D \), has been obtained by decoupling (4) at these conditions, in order to ease the integration. Then, at the depletion region, the total charge is a function of \( \alpha \), as follows:

\[
q_{\text{dep}} = \beta \cdot \sqrt{e^\xi \alpha - \xi \cdot \alpha - 1}
\]

(5)

Whereas in accumulation region, the total charge is a function of \( \psi_s \), which is given as:

\[
q_{\text{acc}} = -\beta \cdot \sqrt{e^\frac{\psi_t - \psi_s}{\gamma} - \psi_s - \psi_t - 1}
\]

(6)

Finally, a continuous mobile charge expression from depletion to accumulation is obtained using the tanh function as follows:

\[
q_{\text{tot}} = \frac{1}{2} q_{\text{dep}} \left[ 1 - \tanh\{25(V_G - (V_{FB} + V_D))\} \right] + \frac{1}{2} q_{\text{acc}} \left[ 1 + \tanh\{25(V_G - (V_{FB} + V_D))\} \right]
\]

(7)

2.3. Drain current

As already mentioned, \( I_D \) is obtained by integrating all of the electron mobile charge inside the silicon layer (4) by:

\[
I_D = 2 \cdot \frac{W}{L} \cdot C_{\text{ox}} \cdot \mu \cdot \int_{V_{FB}}^{V_G} q_t \cdot dV
\]

(8)

Since (4) cannot be integrated in simple mathematical steps, the mobile charges for accumulation and depletion regimes were used. Final expressions of the drain current according to [18] in below threshold, \( I_{\text{dep,bt}} \), as well as in above threshold,
\( I_{\text{dep,at}} \) are equal to:

\[
I_{\text{dep}} = -0.03 \cdot K \cdot \psi_{l}
\]

\[
\left\{ \frac{1}{2} \left( q_{\text{totS}}^{2} - q_{\text{totD}}^{2} \right) + \frac{\beta}{\xi} \left[ SaN(\xi_{S}) - SaN(\xi_{D}) \right] \right\}
\]

(9)

\( I_{\text{dep}} = K \left\{ \frac{q_{b}}{2} [V_{D} - V_{S} + 0.01(1.1 \cdot 10^{-4} - V_{D})] + \frac{\psi_{l}}{2} (q_{\text{totS}}^{2} - q_{\text{totD}}^{2}) + \psi_{l}^{2} \left[ SaP \left( \frac{V_{G} - V_{FB} - V_{S}}{\psi_{l}} + q_{\text{totS}} \right) \right] - \psi_{l} \beta \left[ Sb(V_{G}) - Sb(V_{D}) \right] \right\}
\]

(10)

\[
\mu_{S} = \frac{\mu_{0}}{1 + \left[ \theta_{1}(V_{G} - V_{FB}) + \theta_{2}V_{\text{Deff}} \right] \cdot \frac{1}{2} \left( 1 + \tanh \left[ 5(V_{G} - V_{FB}) \right] \right)}
\]

(15)

where \( q_{\text{totS,D}} = q_{\text{tot}}(V_{G}, V_{S,D}) \), \( \alpha_{S,D} = \alpha(V_{G}, V_{S,D}) \) and \( K = \frac{\mu_{0}}{L C_{\text{in}}} \). As a result, a continuous expression for the drain current in the depletion regime is given by:

\[
I_{\text{dep}} = \frac{I_{\text{dep,at}}}{1 - \tanh[30(V_{G} - V_{T})]} + \frac{1}{2} I_{\text{dep,at}} \left[ 1 + \tanh[30(V_{G} - V_{T})] \right]
\]

(11)

Whereas, the current in the accumulation regime is calculated as:

\[
I_{\text{acc}} = K \left\{ \frac{q_{b}}{2} (V_{D} - V_{S}) + \frac{\psi_{l}}{2} (q_{\text{totS}}^{2} - q_{\text{totD}}^{2}) + \psi_{l} \beta \left[ SaP \left( \frac{V_{G} - V_{FB} - V_{S}}{\psi_{l}} + q_{\text{totS}} \right) \right] - \psi_{l} \beta \left[ Sb(V_{G}) - Sb(V_{D}) \right] \right\}
\]

(12)

Also, expressions for functions \( SaN, Sb, SaP \) are defined in [18]. The final expression for the total drain current valid in both regimes is equal to:

\[
I_{\text{tot}} = \frac{I_{\text{dep}}}{1 - \tanh[100(V_{G} - (V_{FB} + V_{D}))]} + \frac{1}{2} I_{\text{acc}} \left[ 1 + \tanh[100(V_{G} - (V_{FB} + V_{D}))] \right]
\]

(13)

\[ 2.4. Short channel effects \]

The expression for the current (13) is used as the core model for DJLT. With the channel length reduction, 2D effects appear near the source and drain producing the so-called Short Channel Effects (SCE). In our core model, the effects of velocity saturation, channel length modulation, Drain Induced Barrier Lowering (DIBL) and subthreshold degradation were included, describing the process in the following sections:

\[ 2.4.1. Velocity saturation and variable mobility. \] For short channel devices the carrier velocity saturation \( v_{\text{sat}} \) obtained at the critical electrical field along the channel, gives a surface mobility reduction as:

\[
\mu_{\text{eff}} = \frac{\mu_{S}}{\sqrt{1 + \left( \frac{\mu_{S}}{L \cdot V_{\text{sat}}} \right)}}
\]

(14)

where the effective mobility is given by the superposition of two parallel currents: one flowing through the center with a constant mobility \( \mu_{0} \) and the other at the surface of the silicon layer, which presents scattering effects. As a result, surface mobility can be calculated as in [18]:

\[
\mu_{S} = \frac{\mu_{0}}{1 + \left[ \theta_{1}(V_{G} - V_{FB}) + \theta_{2}V_{\text{Deff}} \right] \cdot \frac{1}{2} \left( 1 + \tanh \left[ 5(V_{G} - V_{FB}) \right] \right)}
\]

(15)

where \( \theta_{1} \) and \( \theta_{2} \) are adjusting parameters defining the mobility degradation for \( V_{G} > V_{FB} \). Furthermore, the effective drain voltage \( V_{\text{Deff}} \) as well as the drain saturation voltage \( V_{\text{Dsat}} \) are defined by:

\[
V_{\text{Deff}} = V_{\text{Dsat}} + \frac{1}{2} [V_{D} - V_{\text{Dsat}} + \psi_{l}] - \sqrt{(V_{D} - V_{\text{Dsat}} + \psi_{l})^{2} + 4\psi_{l}V_{\text{Dsat}}}
\]

(16)

\[
V_{\text{Dsat}} = \begin{cases} V_{G} - V_{T0} & \text{for } L \geq 300 \text{ nm} \\ 0.08 + \eta(L_{\text{sat}})^{0.33}(V_{G} - V_{T0}) & \text{for } L < 300 \text{ nm} \end{cases}
\]

(17)

where \( \eta \) is an adjusting parameter. The threshold voltage for long channel transistors is given by:

\[
V_{T0} = V_{FB} - \psi_{l} \left[ \frac{q_{b}}{2} - \frac{1}{4} - \alpha_{T} - \ln \left( 1 - \frac{\alpha_{T}}{\alpha_{tr}} \right) \right]
\]

(18)

\[ 2.4.2. Subthreshold characteristics. \] In subthreshold regime the channel electrostatic potential of the DJLT is obtained by considering that the total charge is approximately equal to the fix charge (full depletion). In order to consider this regime, the subthreshold slope degradation as well as the SCE in the threshold voltage, such as the roll-off and the DIBL, an effective gate voltage, \( V_{\text{Geff}} \), has to be introduced instead of \( V_{G} \), and is expressed as:

\[
V_{\text{Geff}} = V_{G} + \psi_{0 \text{min}} - \psi_{0p}
\]

(19)

where the minimum value of the potential, \( \psi_{0 \text{min}} \), is defined according to [18] by:

\[
\psi_{0 \text{min}} = \psi_{0p} + \frac{\sqrt{2U_{S}U_{D}\cosh \left( \frac{L}{t_{n}} \right) - U_{S}^{2} - U_{D}^{2}}}{\sinh (L/t_{n})}
\]

(20)
where the subthreshold potential at the center of the silicon layer for a long channel device \( \psi_{\text{th}} = V_G - V_{FB} + \frac{q}{\lambda} \), \( \lambda \) is the double gate natural length [5], \( U_g = V_{\text{bias}} - \psi_{\text{th}} \). The built-in effective voltage, considering the effect of source and drain extensions according to [14], is given by:

\[
V_{\text{bias},SD} = \psi_{\text{th}} - \frac{2q_{\text{N},\text{Dest}}}{\lambda} \tag{21}
\]

where \( V_{\text{bias}} = V_A + \psi_f \) is the built-in voltage at the source/channel interface, \( \psi_f \) is the Fermi level in the channel and \( V_A \) is the constant parameter. Finally, threshold voltage roll-off is given through a threshold voltage correction of \( V_T \) as:

\[
\Delta V_T = \frac{V_{\text{bias}} - (V_T - V_{FB} + \frac{q_{\text{N},\text{Dest}}}{\lambda})}{\cosh(L/2\lambda)} \tag{22}
\]

### 2.4.3. Channel length modulation

Another effect produced by the increment in the electrical field along the channel is the channel length modulation (CLM), which is consider as:

\[
\Delta L = \lambda \sqrt{\frac{2e_z}{\mu_0} (V_D - V_{\text{Def}})} \tag{23}
\]

### 2.4.4. Series resistance

The series resistance effect due to the source and drain extensions has been introduced into the current factor \( K \) of (12) as:

\[
KK = \frac{1}{1 - \Delta L/L} \cdot \left( 1 + KR(V_{\text{eff}} - V_T - nV_{\text{Def}}) \cdot \frac{1}{2} \cdot \left[ 1 + \tanh[2(V_G - V_T - nV_{\text{Def}})] \right] \right) \tag{24}
\]

where \( R \) is the sum of the source and drain resistances and \( n \) is the adjusting parameter. The drain current is calculated using the effective gate voltage, the effective drain voltage and \( KK \) instead of \( K \) in expressions (9–12).

### 3. Verilog-A implementation of the DJLT model in circuit simulators

In order to assess the validity of the DJLT model to perform DC circuit simulations, we have implemented the aforementioned equations in Verilog-A language (see appendix A). Thanks to its support for different modules where each one can be described mathematically in terms of its terminals and external parameters applied to the module, Verilog-A language seems to be the best tool for describing compact modeling. The descriptive code of the model was introduced in Ngspice according to [22]. It is worth pointing out that Ngspice is a free circuit simulator to integrate Verilog-A code. However, due to its limited built-in functions and external tools to perform the compilation such as the ADMS interface, a more complex implementation has to be done in order to obtain similar results as in commercial tools, as well as to avoid convergence problems. Validation of the implementation of the DJLT model in Verilog-A was performed through 2D numerical simulations in order to obtain similar results as in [18].

As good practice, it is necessary to define the built-in functions which will be used several times along the code. Those are located at the beginning of the code (lines 9–229). It is worth pointing out that the way the functions are defined can allow the user to compile them either in open source software, such as Ngspice, or in commercial software without making any change. Therefore, the model parameters are listed in lines 240–260 and also shown in table 1.

Furthermore, the difference of the potentials at the threshold voltage (3) is first determined in order to calculate the threshold voltage (lines 371–380). Afterwards, subthreshold behavior is calculated by the effective gate voltage (18) in lines 382 to 394, in which the main SCE are covered. The effective drain voltage is determined due to the saturation velocity (lines 395–414). Once the effective voltages at the drain and gate as well as the threshold voltage are known, it is possible to

#### Table 1. Model parameters and extracted values for model simulations.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>( L ) (( \mu \text{m} ))</th>
<th>( N_{D0} \cdot 10^{10} ) (( \text{cm}^{-3} ))</th>
<th>( \mu_0 ) (( \text{cm}^2/\text{V}\cdot\text{s} ))</th>
<th>( \theta_1 ) (( \text{V}^{-1} ))</th>
<th>( \theta_2 ) (( \text{V}^{-1} ))</th>
<th>( R ) (( \Omega ))</th>
<th>( n )</th>
<th>( \lambda )</th>
<th>( \eta )</th>
<th>( V_{\text{sat}} \cdot 10^2 ) (( \text{cm}^{-1} ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 ( \mu \text{m} )</td>
<td>1</td>
<td>100</td>
<td>(-0.02)</td>
<td>(0.02)</td>
<td>(216)</td>
<td>0.3</td>
<td>(0)</td>
<td>(0.15)</td>
<td>1</td>
<td>(0)</td>
</tr>
<tr>
<td>1 ( \mu \text{m} )</td>
<td>0.5</td>
<td>145</td>
<td>(-0.22)</td>
<td>0.23</td>
<td>530</td>
<td>0.85</td>
<td>(0.75)</td>
<td>(0.142)</td>
<td>0.75</td>
<td></td>
</tr>
<tr>
<td>1 ( \mu \text{m} )</td>
<td>0.5</td>
<td>15</td>
<td>(-0.02)</td>
<td>(0.05)</td>
<td>167</td>
<td>0.7</td>
<td>(0)</td>
<td>(0.118)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>40 ( \text{nm} )</td>
<td>1</td>
<td>98</td>
<td>(0.02)</td>
<td>(0.32)</td>
<td>45</td>
<td>0.86</td>
<td>(0.35)</td>
<td>(0.153)</td>
<td>1.23</td>
<td></td>
</tr>
<tr>
<td>40 ( \text{nm} )</td>
<td>0.5</td>
<td>140</td>
<td>(-0.23)</td>
<td>0.93</td>
<td>60</td>
<td>0.9</td>
<td>(0.24)</td>
<td>(0.136)</td>
<td>1.4</td>
<td></td>
</tr>
<tr>
<td>40 ( \text{nm} )</td>
<td>0.5</td>
<td>15</td>
<td>(-0.02)</td>
<td>(0.05)</td>
<td>33</td>
<td>0.4</td>
<td>(0.28)</td>
<td>(0.112)</td>
<td>1.2</td>
<td></td>
</tr>
</tbody>
</table>
calculate the potentials at the center of the silicon layer and at the surface close to the drain and to the source (lines 415–433). Then, potentials are used to determine the mobile charges in the depletion regime and in accumulation (lines 434–466). Finally, the drain current is calculated (lines 480–506), through considering the effective mobility (lines 467–470), CLM (lines 471–474) and series resistance (lines 475–479).

4. Results and discussion

The implemented description for DJLT in Verilog-A was introduced in the circuit simulator Ngspice. The results obtained from the simulations were compared with ATLAS simulations. Double-gate Junctionless transistors with two different gate lengths (L = 1 µm and 40 nm) with 10 nm or 15 nm of silicon layer thickness and $5 \times 10^{18}$ cm$^{-3}$ or $1 \times 10^{19}$ cm$^{-3}$ doping...
concentration were considered. Also, all simulated transistors have 2 nm gate oxide thickness and 1 μm gate width as well as 5.2 eV work function. Table 1 shows the extracted parameters of the transistors used in Ngspice simulations.

Figure 2 (top) shows the comparison of simulated and modeled transistors in linear normalized transfer characteristic at $V_{DS} = 50$ mV. Furthermore, figure 2 (bottom) shows the semilogarithmic characteristic in order to observe the sub-threshold region. Good agreement from depletion to accumulation is obtained. Also, good agreement between the modeled and simulated transistors is obtained in figure 3 for normalized transfer characteristics at $V_{DS} = 1.5$ V.

Normalized output characteristics are shown in figure 4 for two different gate voltages, whereas normalized transconductance at $V_{DS} = 50$ mV and 1.5 V are shown in figure 5. Finally, normalized conductance at $V_{GS} = 1$ V is shown in figure 6.

As can be seen from linear to saturation conditions, continuous modeled characteristics show good agreement with the simulated data.

## Conclusion

In this work, we present the implementation of the DJLT model in Verilog-A, which considers short channel effects, variable mobility and series resistance. Development and implementation of special subfunctions in Verilog-A were necessary to be performed, such as Lambert and Gauss’s hypergeometric functions, in order to obtain good agreement between analytical expressions and modeled simulations, as well as to obtain fast convergence. The expression for the calculation of the variable mobility, as well as short channel effects that include channel length modulation, DIBL, $V_t$ roll-off, subthreshold variation as well as carrier velocity saturation and series resistance were also implemented. Modeled and simulated transfer characteristics in linear and saturation regions, as well as the output characteristics, show good agreement in all operating regions, which allows us to confirm that the Verilog-A implemented compact analytical model for DJLT presented in this work is able to describe digital and mixed electronic circuits operating in DC.

## Acknowledgments

This work was supported at BUAP by VIEP project No. 275, as well as at CINVESTAV by CONACYT project 236887.

## Appendix A

```verbatim
//JUNCTIONLESS TRANSISTOR

#include "discipline.h"
```

Figure 6. Comparison of simulated (symbols) and model implemented (lines) conductance characteristic at $V_{G} = 1$ V. Open symbols corresponds to 40 nm channel length, and filled symbols to 1 μm.
(Continued.)

7 'include "constants.h"
8 //** Constant **/
9 'define q (1.60219E-19)
10 'define Eo (8.85419E-14)
11 'define ko (3.9)
12 'define kB (1.38066E-23)
13 'define ks (11.8)
14 'define T (300)
15 //** Square Root Function **/
16 'define fssqrt (x1, fsqrt1)\n17 if (x1>0)\n18  fsqrt1=sqrt (x1);\n19 else\n20  fsqrt1=0;\n21 //** Sign Function **/
22 'define fsign(datain,sgn)\n23 if (datain==0)\n24  sgn=0;\n25 else\n26  sgn=datain/abs(datain);\n27 //** Lambert Function **/
28 'define flambert(z,w)\n29 if(z>0)\n30  fl11=1;\n31 else\n32  fl1=0;\n33 tmpln=ln(fl1+z);\n34 'fssqrt(2*(exp1+z+1),flam1);\n35 if(tmpln>0)\n36  w=tmpln - ln(tmpln);\n37 else\n38  w=flam1 - 1;\n39  kl=1;\n40 while (kl<=26) begin \n41   c11=exp(w);\n42   c21=w* c11 - z;\n43   if(w!= 1) begin\n44       fl21=1;\n45   end else begin\n46      fl21=0;\n47   end\n48   w1=w + fl21;\n49   dwl=c21/(c11* w1 - 0.5 * ((w + 2) *\n50      (c21 / w1) ));\n51  w=w - dwl;\n52  kl=kl+1;\n53 end
54 //** Surface Potential calculation through 3th order Newton-Raphson **/
55 'define fht(ht,Vg,Vth,Vx,htBeta,htepsilon,htVd, \n56    htphiht,htB)\n57 fhtx1 = htB* exp(htx1);\n58 'flambert(htF1,htx2);\n59 'fsgn(htBeta,htx3);\n60 'fssqrt((htx3+htBeta)*htx4)-1,htx4)\n61 ft=htx1+((htx1*htBeta)+htx4)/(htx1*(htVd+htVd))/htpht;\n62 'flambert(htB*exp(htx5),htx5);\n63 'flambert(htB*exp(htx6),htx6);\n64 'fsgn(2*htBeta,htx7);\n65 'fssqrt(exp(htx)-htepsilon-1,htx8);\n66 ft1=1+((htBeta+htx7)/2)*((exp(htx)+htepsilon+htBeta1)/( \n67    htVd));\n68 'flambert(httheta*exp(htx9),htx9);\n69 'flambert(httheta*exp(htx10),htx10);\n70 alpha2=htx9/pow(1+htx10,3);\n71 'fsgn(2*htBeta,htx11);\n72 'fssqrt((htx)-htepsilon*htBeta1,htx12);\n73 'flambert(httheta*exp(htx13),htx13);\n74 'flambert(httheta*exp(htx14),htx14);\n75 'flambert(httheta*exp(htx15),htx15);\n76 alpha3=htx13/(1+2*htx14)/pow(1+htx15,5.5);\n77 'fsgn(2*htBeta,htx16);\n78 'fssqrt(exp(htx)-htepsilon-1,htx17);\n79 f3=-(htBeta+htx16)/2)/((-exp(htx)+htepsilon*htBeta3)/ \n80    (=htx17)+3/2)*((exp(htx)-htepsilon*htBeta1+(exp(htx) \n81    -htepsilon*htBeta2)/pow(exp(htx)-htepsilon*htBeta1 \n82     -1.55)/3*(pow(exp(htx)-htepsilon*htBeta1,3)/pow(exp( \n83    htVd))/htepsilon-HTalpah*1.55));\n84 rht=-(ft+1+(1/(fhtx2)+2*(pow(fhtx1,2))))+(fhtx1)/( \n85    (fhtx1,4))+(3*(pow(2,2)-fhtx1));\n86 //** XTC Init **/
87 'define fxtc(xtcVg,xtcVd,xtcVth,xtcAlpha,xtcBeta, \n88    xtcF,xtcError,xtcBeta,xtcLambda,xtcPhi,xtcN);\n89 xtcpmax=xtcBeta*xtcLambda*xtcPhi,xtcN;\n90 xtcBeta=xtcBeta*xtcLambda*xtcPhi,xtcN;\n91 xtcVd=xtcBeta*xtcLambda*xtcPhi,xtcN;\n92 xtcAlphas=xtcBeta*xtcLambda*xtcPhi,xtcN;\n93 xtcBeta=xtcBeta*xtcLambda*xtcPhi,xtcN;\n94 xtcVd=xtcBeta*xtcLambda*xtcPhi,xtcN;\n95 xtcError=xtcBeta*xtcLambda*xtcPhi,xtcN;\n96 xtcBeta=xtcBeta*xtcLambda*xtcPhi,xtcN;\n97 xtcVd=xtcBeta*xtcLambda*xtcPhi,xtcN;\n98 xtcError=xtcBeta*xtcLambda*xtcPhi,xtcN;\n99 xtcBeta=xtcBeta*xtcLambda*xtcPhi,xtcN;\n100 xtcVd=xtcBeta*xtcLambda*xtcPhi,xtcN;\n101 xtcError=xtcBeta*xtcLambda*xtcPhi,xtcN;\n102 xtcBeta=xtcBeta*xtcLambda*xtcPhi,xtcN;\n103 xtcVd=xtcBeta*xtcLambda*xtcPhi,xtcN;\n104 xtcError=xtcBeta*xtcLambda*xtcPhi,xtcN;\n105 xtcBeta=xtcBeta*xtcLambda*xtcPhi,xtcN;\n106 xtcVd=xtcBeta*xtcLambda*xtcPhi,xtcN;\n107 xtcError=xtcBeta*xtcLambda*xtcPhi,xtcN;
209 \[ f_{txtc}(Sbtaux2, Sbtx, SbtVb, SbtxV, Sbtxtalphaus, SbtB, SbtxBeta, Sbtxepsion, Sbtphit, Sbtq, SbtNd, SbtEs, Sbtlambda0, Sbtxtc04); \]
210 \[ 'falfa(Sbttalphaus, SbtB, Sbtxtc04, Sbttaflu04); \]
211 SbtA40= ’Sbtxepsion ’
212 \[ + \] Sbtaflu04; \\
213 \[ 'fSbtxA02, SbtxJt3aux3); \]
214 \[ 'fSbtxA04, SbtJt2aux5); \]
215 Sbt=xSbtaux3 \( + (\text{Sbtaux3-1}) \times 0.5 \) \( \text{SbtVg} \) \( - (\text{SbtVt} \)
216 \[ \text{SbtVd}, \text{SbtVs}; \]
217 \[ //** Final Sel Solution called S3x **// \]
218 \[ \text{define fS3x}(S3xVg, S3xVd, S3xVs, S3xVf, S3xVt, S3xalphaus, S3xB, S3xBeta, S3xepsion, S3xphit, S3xq, S3xNd, S3xEs, S3xlambda0, S3x00, rS3x); \]
219 \[ if \ (S3xVt < -0.25)) \] \( \text{begin} \)
220 \[ 'fSbtx(S3xVg, S3xVd, S3xVs, S3xVf, S3xVt, S3xalphaus, S3xB, S3xBeta, S3xepsion, S3xphit, S3xq, S3xNd, S3xEs, S3xlambda0, S3x00, rS3x); \]
221 \[ end \] \( \text{begin} \)
222 \[ 'ftxtc(S3xVg, S3xVd, S3xVs, S3xVf, S3xVt, S3xalphaus, S3xB, S3xBeta, S3xepsion, S3xphit, S3xq, S3xNd, S3xEs, S3xlambda0, S3x00, rS3x); \]
223 \[ 'falfa(S3xalphaus, S3xB, S3xBeta, S3xepsion, S3xphit, S3xq, S3xNd, S3xEs, S3xlambda0, S3x00, rS3x); \]
224 \[ \text{end} \] \( \text{begin} \)
225 \[ //** Subx Function **// \]
226 \[ \text{define fSubx(x,0.1 Subx)} \]
227 \[ 'fSqrt((-1-x), Subxvar1); \]
228 \[ 'fSqrt(abs(1+0), Subxvar2); \]
229 \[ \text{Subx} = -2*(Subxvar1 - Subxvar2*atan(Subxvar1/} \]
230 \[ \text{Subxvar2}); \]
231 \[ 230 \]
232 \[ 231 \]
233 \[ 232 \]
234 \[ 233 \]
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236 \[ 235 \]
237 \[ 236 \]
238 \[ 237 \]
239 \[ 238 \]
240 \[ \text{parameter real Npoly = 1E20 from [0.0:inf]);} \]
241 \[ \text{parameter real L = 1000E-7 from [0.0:inf]);} \]
242 \[ \text{parameter real ts = 10E-7 from [0.0:inf]);} \]
243 \[ \text{parameter real Nss = 5E10 from [0.0:inf]);} \]
244 \[ \text{parameter real Hfin = 1E-4 from [0.0:inf));} \]
245 \[ \text{parameter real Ndxet = 1E20 from [0.0:inf));} \]
246 \[ \text{parameter real Lext = 30E-7 from [0.0:inf));} \]
247 \[ \text{parameter real WW = 1E-4 from [0.0:inf));} \]
248 \[ \text{parameter real Nd = 1E19 from [0.0:inf));} \]
249 \[ \text{parameter real P1 = -0.015 from [-inf:inf]);} \]
250 \[ \text{parameter real uo = 100 from [0.0:inf));} \]
251 \[ \text{parameter real R = 216 from [0.0:inf));} \]
252 \[ \text{parameter real n = 0.3 from [0.0:inf));} \]
253 \[ \text{parameter real theta1 = -0.02 from [-inf:inf));} \]
254 \[ \text{parameter real theta2 = 0.02 from [-inf:inf));} \]
255 \[ \text{parameter real vsat = 1E7 from [0.0:inf));} \]
256 \[ \text{parameter real lambda = 0 from [0.0:inf));} \]
257 \[ \text{parameter real Eta = 0.15 from [0.0:inf));} \]
258 \[ \text{parameter real phimet = 5.198 from [0.0:inf));} \]
259 \[ \text{parameter real to = 2E-7 from [0.0:inf));} \]

(Continued.)

260 \[ \text{parameter real Va = 0.75 from [0.0:inf]);} \]
261 \[ \text{parameter real \( \alpha \)} \]
262 \[ \text{parameter real \( \gamma \)} \]
263 \[ \text{parameter real \( \delta \)} \]
264 \[ \text{parameter real \( \epsilon \)} \]
265 \[ \text{parameter real \( \zeta \)} \]

(Continued.)
314 //** Bandgap ***/
315 'fssqrt(pwln(Nd/(1E17),2))+(0.5,Vx1);
316 DEg=-(9E-3)+(pwln(1E17)+Vx1);
317 Ego=1.08+(4.73E-4)*(pwln(300,2)/(300+636))-
318 (pw(T,2)/(T+636));
319 Eg=Ego-DEg;
320 phiEgEg=-Eg;
321 'fssqrt(pwln(Npoly/(1E17),2)+0.5,Vx1);
322 DEgpp=(9E-3)+(pwln(1E17)+Vx1);
323 Ego=1.08+(4.73E-4)*(pwln(300,2)/(300+636))-
324 (pw(T,2)/(T+636));
325 Ego=Ego-DEgpp;
326 phiEgpp=-Egpp;
327 //** Density of States ***/
328 Nc=2.8E19*powl(T,300,1.5);
329 Nv=1.04E19*powl(T,300,1.5);
330 'fssqrt(Nc=Nv,Vx1);
331 //** Intrinsc Concentration ***/
332 ni=Vx1*powl(-(Eg/2)+phiits);
333 ai=ln(ni);
334 niep=Vx1*powl(-(Eg/2)+phiits);
335 //** Fermi Level in the Silicon ***/
336 phif=phi-ln(Nd/ni);
337 Ef=phi;
338 //** Fermi Level in Poly ***/
339 phip=phi-ln(Npoly/niep);
340 Efip=phi-
341 //** Intrinsic Level ***/
342 Ei=0.5*Eg+(0.5*phiit-ln(Nv/Nc));
343 phiit=-Ei;
344 Eip=0.5*Egp+(0.5*phiit-ln(Nv/Nc));
345 phiit-Eip;
346 //** Fermi Level in Extensions ***/
347 phifext=-phiit-ln(Ndnext/ni);
348 //** Capacitances ***/
349 Co=Eox/au;
350 Cs=Es/au;
351 //** Ion Concentrations ***/
352 Qb='q*Nd/au;
353 qb='q/(Co/phiit);
354 //** Charging Interface ***/
355 Qn='q*Nn;
356 //** Extractive Work ***/
357 xef=4.17+DEg+0.5;
358 phisem=+Egp+0.5+phiit;
359 phism=phim-
360 phisms=phiit-ln(Npoly*Nd/(ni+niep));
361 //** Flat Band Voltage ***/
362 phms=phism;
363 Vb=phims-(Qb/Co);
364 //** Auxiliary Relationships ***/
365 delta=Cx/(Co+Cx);
366 gamma=Co/(4*Cx);
367 'fssqrt(Es/(2*Eox)+to+ts),tn);
368 'fssqrt(2,txn);
369 'fssqrt(1+(4*Cx/Co),Vx2);
370 tnA=+(2*Vx1)*Vx2;
371 P0=phiit;
372 //** Difference of Potentials in Deep Subthreshold ***/
373 phidus=-Qb/(8*Cs);
374 alphasu=phidus/phiit;
(Continued.)
373 //** Threshold Voltage ***/
374 alphal=alphal/(1-alphal)*(1-alphal+pow
375 alphal=alphal/(1-(1-2/qb),2));
376 Vt=Vfb+phiit(qb2-0.25-alphal-ln(1-alphal/alphal));
377 //** Natural Length Double Gate ***/
378 'fssqrt(Es/(2+Eox+1-((Eox+ts)/(4+to)))*st+to),
379 Vbis=Va+phiit;
380 //** Potential Barrier Change Described by Phim ***/
381 if (V(s) < Vt) begin
382 'deltaf alphamin(Vg),Vfb,Vd),q,Nd,Es,lambd,ab,abis,ndex,
383 end else begin
384 'deltaf alphamin(Vt,Vfb,Vd),q,Nd,Es,lambd,ab,abis,
385 end
386 'deltaf alphamin(Vt,Vfb,Vd),q,Nd,Es,lambd,ab,abis,
387 end
388 'deltaf alphamin(Vt,Vfb,Vd),q,Nd,Es,lambd,ab,abis,
389 end
390 'deltaf alphamin(Vt,Vfb,Vd),q,Nd,Es,lambd,ab,abis,
391 end
392 //** Effective Voltage VGS ***/
393 aux1=deltaf alphamin(Vg)=0.5*(1-tanh(50*(V
394 aux2=deltaf alphamin(Vt+Vg))=0.5*(1-tanh(50*(V
395 Vgef=aux2+aux2;
396 //** Saturation Voltage ***/
397 Vsat0=Vgef-Vt;
398 Vsat1=0.08+Etau(pwL+vsat,0.33)+(Vgef-Vt);
399 //** Transition between Vdsat ***/
400 Vgtrans=((0.08)/(1-Etau(pwL+vsat,0.33)))+(Vg-trans);
401 //** Saturation Voltage ***/
402 var1=Etau(pwL+vsat,0.33));
403 if (var1 >= 1) begin
404 Vdsat=Vsat1+(0.5)+(1-tanh(2*(Vgef-Vgtrans))
405 +Vsat0+(0.5)+(1-tanh(2*(Vgef-Vgtrans))
406 end else begin
407 Vdsat=Vsat1+(0.5)+(1-tanh(2*(Vgef-Vgtrans))
408 end
409 end
410 if (L >= 200) begin
411 Vdsat=Vsat0;
412 end
413 //** Effective Saturation Voltage ***/
414 'fssqrt(powl(Vd-Vdsat+P0,2))/(8+Vdsat+P0),
415 Vdef=Vdsat+(0.5*(Vd-Vdsat+P0))
416 'ffsqrt1(Vd);
417 //** Effective Drain Voltage ***/
418 Vdvs=(Vd)+0.5*(1-tanh(Vgef-Vgtrans+15)))+(Vdef+(0.5*(1
419 +tanh(Vgtrans-Vt)))
420 //** Potential at the Center ***/
421 fiop=Vgef-Vfb+(q*Nd)/(Es)pow(lambd,ab,2);
422 //** Difference of Potentials ***/
423 alphasur=alphasur+1-exp((fiop-Vdvs)/phiit);
424 alphasur=alphasur+1-exp((fiop-Vdvs)/phiit);
425 //** Surface Potential ***/
426 //** Bandgap ***/
427 'fssqrt(pwln(Nd/(1E17),2)+0.5,Vx1);
428 DEg=-(9E-3)+(pwln(1E17)+Vx1);
429 Ego=1.08+(4.73E-4)*(pwln(300,2)/(300+636))-
430 (pw(T,2)/(T+636));
431 Eg=Ego-DEg;
432 phiEgEg=-Eg;
433 'fssqrt(pwln(Npoly/(1E17),2)+0.5,Vx1);
434 DEgpp=(9E-3)+(pwln(1E17)+Vx1);
435 Ego=1.08+(4.73E-4)*(pwln(300,2)/(300+636))-
436 (pw(T,2)/(T+636));
437 Ego=Ego-DEgpp;
438 phiEgpp=-Egpp;
439 //** Density of States ***/
440 Nc=2.8E19*powl(T,300,1.5);
441 Nv=1.04E19*powl(T,300,1.5);
442 'fssqrt(Nc=Nv,Vx1);
443 //** Intrinsc Concentration ***/
444 ni=Vx1*powl(-(Eg/2)+phiits);
445 ai=ln(ni);
446 niep=Vx1*powl(-(Eg/2)+phiits);
447 //** Fermi Level in the Silicon ***/
448 phif=phi-ln(Nd/ni);
449 Ef=phi;
450 //** Fermi Level in Poly ***/
451 phip=phi-ln(Npoly/niep);
452 Efip=phi-
453 //** Intrinsic Level ***/
454 Ei=0.5*Eg+(0.5*phiit-ln(Nv/Nc));
455 phiit=-Ei;
456 Eip=0.5*Egp+(0.5*phiit-ln(Nv/Nc));
457 phiit-Eip;
458 //** Fermi Level in Extensions ***/
459 phifext=-phiit-ln(Ndnext/ni);
460 //** Capacitances ***/
461 Co=Eox/au;
462 Cs=Es/au;
463 //** Ion Concentrations ***/
464 Qb='q*Nd/au;
465 qb='q/(Co/phiit);
466 //** Charging Interface ***/
467 Qn='q*Nn;
468 //** Extractive Work ***/
469 xef=4.17+DEg+0.5;
470 phisem=+Egp+0.5+phiit;
471 phisms=phim-
472 phisms=phiit-ln(Npoly*Nd/(ni+niep));
473 //** Flat Band Voltage ***/
474 phms=phism;
475 Vb=phims-(Qb/Co);
476 //** Auxiliary Relationships ***/
477 delta=Cx/(Co+Cx);
478 gamma=Co/(4*Cx);
479 'fssqrt(Es/(2*Eox)+to+ts),tn);
480 'fssqrt2,txn);
481 'fssqrt(1+(4+Cx/Co),Vx2);
482 tnA=+(2*Vx1)*Vx2;
483 P0=phiit;
484 //** Difference of Potentials in Deep Subthreshold ***/
485 phidus=-Qb/(8*Cs);
486 alphasu=phidus/phiit;
(Continued.)
421 psaprox=alphaaprox+phi1+phi2;
422 psaproxS=alphaaproxS+phi1+phi2;
423 // ** Calculated Surface Potential /**
424 'ftxc(Vgef,Vdefs,Vfb,Vt,alphasu,B,Beta,epsilon,phi1,Nd,
425 lambdao, x);
426 'fps(x, phi,Vdef,psC);
427 // ** Calculated Difference of Potentials /**
428 'ftaIn(alphasu,B, x,lambdao);
429 // ** Potential Calculated at the Center /**
430 poC=psC-phi1+alphaC;
431 'ftxc(Vgef,v(s),Vfb,Vt,alphasu,B,phi1,epsilon,phi1,Nd,
432 Es,lambdao, x, S);
433 'fps(x,S,phi,v(s),psCS);
434 // ** Mobile Charges /**
435 'fsqrt(exp(epsilon+alphaC)-(epsilon+alphaC)-1,fsqrt2);
436 'fsqnt(alphaC,fsqnt1);
437 q1a=-(fsqnt1+Beta)*fsqnt2;
438 'fsqnt(exp(epsilon+alphaC)-(epsilon+alphaC)-1,fsqnt3);
439 'fsqnt(alphaC,fsqnt2);
440 q1a=-(fsqnt1+Beta)*fsqnt3;
441 'fsqnt(abs(-1*(epsilon+alphaC))-1),fsqnt4);
442 'fsqnt(alphaC,fsqnt3);
443 q1b=-(fsqnt3+Beta)*fsqnt4;
444 'fsqnt(abs(-1*(epsilon+alphaC))-1),fsqnt5);
445 'fsqnt(alphaC,fsqnt4);
446 q1bS=-(fsqnt4+Beta)*fsqnt5;
447 q1a=q1a-qb/2;
448 q1bm=q1b-qb/2;
449 q1ams=q1aS-qb/2;
450 q1bms=q1bS-qb/2;
451 'fsqnt(exp(x, x, -1),fsqnt6);
452 'fsqnt(alphaC,fsqnt5);
453 q2=-(fsqnt5+Beta)*fsqnt6;
454 'fsqnt(exp(x, x, -1,fsqnt7);
455 'fsqnt(alphaC,fsqnt6);
456 q2S=-(fsqnt6+Beta)*fsqnt7;
457 q2m=q2-qb/0.5;
458 q2mS=q2S-qb/0.5;
459 q1=(q1bS+0.5)*(1-tanh((Vgef-(Vt+Vdefs)))+
460 (q1aS+0.5)*(1-tanh((Vgef-(Vt+Vdefs)))));
461 q1S=(q1bS+0.5)*(1-tanh((Vgef-(Vt+Vdefs)))+
462 (q1aS+0.5)*(1-tanh((Vgef-(Vt+Vdefs))));
463 qt=(q1S+0.5)*(1-tanh((Vgef-(Vt+Vdefs)))+
464 q2S+0.5) *
465 qtm=qt-qb/0.5;
466 qtmS=qtS-qb/0.5;
467 // ** Mobility /**
468 us=uo/(1+((theta1*(Vgef-Vfb)+theta2*Vdef)*1/2*(1+
469 tanh((5*(Vgef-Vfb))))));
469 'fsqnt(1+(pow((1+Vdef)/(Vsat)),2)),fsqnt8);
470 ues=us/(fsqnt8);
471 // ** shortening channel /**
472 'fsqnt((2+Es)/(q1Nd)+(Vd-Vdefs)),fsqnt9);
473 deltaL=lambdao+fsqnt9;
474 VL=1/(1-deltaL/L);
475 // ** Series resistance /**
476 Ko=2+WW/L+Co;
477 F=ufs/(1+(R*Ko+ufs)*(Vgef-Vt-n*Vdefs)+0.5*(1+tanh(2*(Vgef-Vt-n*Vdefs))));
478 FF=Fs*VL;
479 KK=Ko+phit+FF;
480 // ** Drain Current /**
481 // ** Drain Current in Depletion Region /**
482 D0x=qb-2*(Vdef-V(s));
483 D11x=phit/(2)+((q1S+0.5)*qt);
484 'fSaN(epsilon+alphaC,epsilon+alphaC);
485 'fSaN(epsilon+alphaC,epsilon+alphaC);
486 D12x=(phit(Beta,epsilon) * (fSaN1 — fSaN2);
487 'fS3x(Vgef,Vdefs,V(s),Vfb,Vt,alphasu,B,epsilon,phit,
488 qNd,Es,lambdao,epsilon0, S3x);
489 'fS3x(Vgef,V(s),Vfb,Vt,alphasu,B,epsilon,phit,'q,
488 Es,lambdao,epsilon0, S3x);
489 D13x=(phit(Beta,epsilon) * (fSaN1 — fSaN2);
490 D13x=(-(phit(Beta) *(S3x3 — S3x1))/((Vd)
491 +0.013)+0.01);
492 'fSubs(epsilon+alphaC,epsilon0,fSubx1);
493 'fSubs(epsilon+alphaC,epsilon0,fSubx2);
494 D14x=beta*phit *(fSubx1 — fSubx2);
495 D1subx=—(D11x+D12x+0.034);
496 D1atx=D0x+(P1(1.1e-4*Vdefs))+D11x+D12x+D13x;
497 D1x=(D1subx+0.5*(1-tanh(5*(Vgef-Vt)))+D1atx+0.5*(1
498 +tanh(5*(Vgef-Vt))));
499 // ** Drain Current in Accumulation Region /**
500 SaPaux1=(Vgef-Vb-Vdefs)/phit + q;
501 'fSaP(SaPaux1, S22x);
502 SaPaux2=(Vgef-Vb(V(s)))/phit + qS;
503 'fSaP(SaPaux2, S22x);
504 D22x=phit*Beta*(S22x-S22x);
505 D22x= — D2x + 0.1 + phit*Beta*(S22x-S22x);
506 // ** General Solution in Both Regions /**
507 Dc=D1x+0.5*(1-tanh(20*(Vgef-Vt))); +
508 D2x+0.5*(1
509 +tanh(20*(Vgef-Vt))); +
510 IA=KK*Dx;
511 if(d) <= 1A;
512 end
513 endmodule
References


